**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

**Claims 1-20 (canceled)**

**Claim 21 (new):** A semiconductor device design method for forming a semiconductor device by combining and placing previously registered functional blocks, and determining a wiring pattern in accordance with given logical circuit specifications, and design method comprising:

a registration step of previously registering a first functional block having a first conduction type diode comprising a first conduction type diffusion layer connected to an input pin of the functional block, and a second conduction type well connected to a second power supply or a second conduction type diode comprising a second conduction type diffusion layer connected to the input pin and a first conduction type well connected to a first power supply and a second functional block having the same logic as and the same drive capability as the first functional block but not containing the first or second conduction type diode;

a determination step of determining whether or not a wiring conductor conducting to the input pin and a gate

electrode becomes an antenna ratio exceeding an allowed antenna ratio in said semiconductor device; and

a selection step of selectively using the first functional block, if said determination step determines that the input pin conducts to the gate electrode exceeding the antenna ratio.

**Claim 22 (new):** A semiconductor device formed by combining and placing previously registered functional blocks, and determining a wiring pattern in accordance with given logical circuit specifications, said semiconductor device comprising:

a first functional block including at least one of:

a first conduction type diode having a first conduction type diffusion layer connected to an input pin of the first functional block and a second conduction type well connected to a second power supply, and

a second conduction type diode having a second conduction type diffusion layer connected to the input pin and a first conduction type well connected to a first power supply; and

a second functional block including the same logic as the first functional block but not containing said first or second conduction type diode,

wherein either the first functional block or the second functional block is selectively used depending on

whether or not a wiring conductor conducting to the input pin and a gate electrode becomes an antenna ratio exceeding an allowed antenna ratio in said semiconductor device.

**Claim 23 (new):** A semiconductor device design method for forming a semiconductor device by combining and placing previously registered functional blocks, and determining a wiring pattern in accordance with given logical circuit specifications, and design method comprising:

a registration step of previously registering a first functional block having a first conduction type diode comprising a first conduction type diffusion layer connected to an input pin of the functional block, and a second conduction type well connected to a second power supply or a second conduction type diode comprising a second conduction type diffusion layer connected to the input pin and a first conduction type well connected to a first power supply and a second functional block having the same logic as the first functional block but not containing the first or second conduction type diode;

a determination step of determining whether or not a wiring conductor conducting to the input pin and a gate electrode becomes an antenna ratio exceeding an allowed antenna ratio in said semiconductor device; and

a selection step of selectively using the first functional block, if said determination step determines

that the input pin conducts to the gate electrode exceeding the antenna ratio.

**Claim 24 (new):** A computer-readable recording medium storing the semiconductor device design method as claimed in claim 23 as a program for causing a computer to execute the semiconductor device design method.

**Claim 25 (new):** A semiconductor device design support system for automatically forming a semiconductor device by combining and placing previously registered functional blocks, and determining a wiring pattern in accordance with given logical circuit specifications, said design support system comprising:

registration means for previously registering a first functional block having a first conduction type diode comprising a first conduction type diffusion layer connected to an input pin of the functional block, and a second conduction type well connected to a second power supply or a second conduction type diode comprising a second conduction type diffusion layer connected to the input pin and a first conduction type well connected to a first power supply and a second functional block having the same logic as the first functional block but not containing the first or second conduction type diode;

determination means for determining whether or not a wiring conductor conducting to the input pin and a gate electrode becomes an antenna ratio exceeding an allowed antenna ratio in said semiconductor device; and

selection means for selectively using the first functional block, if said determination step determines that the input pin conducts to the gate electrode exceeding the antenna ratio.